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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/016,693	10/30/2001	Michael D. Lammert	12-1233	2474

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PATENT ADMINSTRATOR
KATTEN MUCHIN ZAVIS ROSENMAN
525 WEST MONROE STREET
SUITE 1600
CHICAGO, IL 60661-3693

EXAMINER	
MALDONADO, JULIO J	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/016,693	LAMMERT, MICHAEL D.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *13-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20040809*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-12 in the reply filed on 07/19/2004 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4, 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kano (U.S. 5,380,679) in view of Lin (U.S. 5,929,525).

In reference to claims 1 and 7, Kano (Figs.2A-2G) in a related method to form interconnect structures teaches providing a substrate layer (1); forming a lower level layer (2) on said substrate layer, selected from one or more of the group consisting of dielectric, metal and circuit devices; forming a seed layer (3) on top of said lower level layer; forming a lower metal layer (5) on said seed layer (4); forming, one or more pillars (8) from a photoresist having top surfaces on said lower metal layer (5), defining photoresist pillars (8); plating said photoresist pillars (8) defining plated pillars (10); removing the seed layer (3) not under the lower level layer; forming a dielectric layer (7); and forming a metal layer (12, 13) over said dielectric layer (11), the metal layer (12, 13) contacting an exposed top surface of said plated pillars (10) (column 4, line 17 – column 5, line 57).

Kano fails to teach coating said one or more plated pillars and said seed layer with a low dielectric polymer; curing said polymer; exposing said top surfaces of said dilated pillars; and forming a metal layer to contact said exposed top surfaces of said plated pillars. However, Lin (Figs.1-9) in a related method to form an interconnect structure teaches the steps of providing a substrate layer (1); forming a lower level layer on said substrate, selected from one or more of the group consisting of dielectric, metal and circuit devices; forming a lower metal layer (9) on said devices (2-7); forming one or metal pillars (12) having top surfaces on said lower metal layer (9); coating said one or more metal pillars with a silicon based dielectric polymer (14); curing said polymer (14); exposing said top surfaces of said metal pillars (12); and forming a metal layer (16) to contact said exposed top surfaces of said metal pillars (11) (column 2, line 50 – column 5, line 23). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kano and Lin to perform the dielectric coatings of Lin to arrive to the claimed invention, and furthermore to roughly planarize the existing topography by filling the spaces between metal pillars (column 4,lines 23 – 37).

In reference to claims 4 and 5, the combined teachings of Lin and Kano teach applying a dielectric layer to said pillars and said metal layer prior to applying said low dielectric polymer, wherein said dielectric layer comprises SiO_2 (Lin, column 2, line 50 – column 5, line 23).

4. Claims 2, 6, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kano ('679) in view of Lin ('525) as applied to claims 1, 4, 5 and 7 above, and further in view of the Applicants' Admitted Prior Art.

Kano in combination with Lin substantially teach applying a dielectric layer to said pillars and said metal layer prior to applying said low dielectric polymer, wherein said dielectric layer comprises SiO_2 (Lin, column 2, line 50 – column 5, line 23), but fail to teach wherein said applying of said dielectric layer comprises applying Si_3N_4 to the coated pillars; and coating the lower metal layer and the plated pillars with a material selected from the group including benzocyclobutene and polynorbornene. However, the submitted prior art teaches applying wherein in practical applications, a polymer such as benzocyclobutene and polynorbornene, is known to be coated over a conventional dielectric, such as silicon dioxide or silicon nitride, on a wafer with metal layers and other topology formed thereon (page 1, [0003] – page 3, [0008]). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Kano and Lin with the prior art to enable the applying and coating step of Kano and Lin to be performed according to the teachings of the prior art because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed x step of refA and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kano ('679) in view of Lin ('525) as applied to claims 1, 4, 5 and 7 above, and further in view of Sonego et al. (U.S. 6,239,042 B1).

The combination of Kano and Lin teach coating with a low-dielectric polymer, non planarizing polymer on the plated pillars and the lower metal layer (Lin, column 2, line 50 – column 5, line 23), but fail to teach forming a planarizing coating over said non-planarizing polymer. However, Sonego et al. in a method to form a dielectric stack teach forming a planarizing coating over a non-planarizing dielectric layer (column 5, lines 44-55). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Kano and Lin with the teachings of Sonego et al. to enable forming the planarizing layer as taught by Sonego et al. in the interconnect formation method of Kano and Lin, since this would improve the planar connection of metal layers (Sonego et al., column 1, lines 16 – 35).

6. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kano ('679) in view of Lin ('525) as applied to claims 1, 4, 5 and 7 above, and further in view of Furukawa et al. (U.S. 6,387,783 B1).

The combined method of Kano and Lin teach using a photoresist to form the plated pillars but fail to expressly teach using a photoresist with a re-entrant profile and using a negative i-line resist. However, Furukawa et al. (Figs.2A-2E) in a related method to pattern a metal layer teach using a photoresist (201) with a re-entrant profile and using a negative i-line resist (column 1, line 43 – 65). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to

combine the teachings of Kano and Lin to enable using a photoresist as taught by Furukawa et al. in the interconnect formation method of Kano and Lin, since this would improve linewidth control in a multilayered stack (column 1, lines 25 – 33).

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kano ('679) in view of Lin ('525) and Furukawa et al. ('783 B1) as applied to claims 1, 4, 5, 7, 10 and 11 above, and further in view of Samoto (U.S. 5,583,063).

Kano in combination with Lin and Furukawa et al. teach using a negative photoresist to define a pattern (Furukawa et al., column 1, line 43 – 65) but fail to expressly teach using a NH_3 image reversal of a photoresist. However, Samoto (Figs.2A-2H) in a related to define a pattern for a semiconductor device teaches using a NH_3 image reversal of a photoresist (column 4, lines 18 – 36). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the photoresist of Samoto in the interconnect formation method of Kano, Lin and Furukawa et al., since this would allow the formation of defined small-sized patterns (column 2, lines 47-50).

Response to Arguments

8. Applicant's arguments filed 11/28/2003 have been fully considered but they are not persuasive.

Applicants argue, "...The Applicant agrees that the Kano patent fails to teach coating of the plated pillars. Paragraph 5 states that the Lin patent discloses "coating said one or more metal pillars with a silicon based dielectric polymer (14)", identified in column 4 of the Lin patent, line 26 et seq., as SOG...SOG has a relatively high dielectric

value and thus increases the capacitance and decreases the performance of the device. For these reasons...the Examiner is respectfully requested to 'reconsider and withdraw this rejection...". In response to this argument, instant paragraphs [0028], [0029], [0025] and [0037] of the submitted disclosure teach coating the plated pillars with a silicon-based polymer. Furthermore, the applicants' admitted prior art teaches using silicon-based polymers as a low dielectric constant polymer (instant paragraph [0003]). Therefore, since the SOG layer is a silicon-based polymer, the Lin reference reads upon that limitation.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (571) 272-1855. The fax number for this group is 703-872-9306 for before final submissions, 703-872-9306 for after final submissions and the customer service number for group 2800 is (703) 306-3329. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

Julio J. Maldonado
September 28, 2004

George Fourson
Primary Examiner